Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	"6615331".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 16:05
S2	2248	(diminish$3 lower$3 (bring$3 adj down) minimiz$3) near5 (cycle adj time)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 16:32
S3	0	S2 same ((column adj redundancy adj check) (column near3 redundan$2))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 16:36
S4	9	(column adj redundancy adj check)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 16:29
S5	168	("6430642" "4654778" "5860026" "6631443" "0182516" "0204649" "0221077" "0128453" "2353122")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 16:32
S6	22	("6430642" "4654778" "5860026" "6631443" "0182516" "0204649" "0221077" "0128453" "2353122"). pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 16:32
S7	31	S4 S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 16:32
S8	0	S7 same (diminish$3 lower$3 (bring$3 adj down) minimiz$3) near5 (cycle adj time)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 16:33

S9	0	S7 and (diminish$3 lower$3 (bring$3 adj down) minimiz$3) near5 (cycle adj time)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 16:34
S10	2	S7 and ((diminish$3 lower$3 (bring$3 adj down) minimiz$3 reduc$3) near5 (cycle adj time))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 16:34
S11	2	S7 and ((diminish$3 lower$3 (bring$3 adj down) minimiz$3 reduc$3) with (cycle adj time))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 16:34
S12	140	S2 and ((column adj redundancy adj check) (column near3 redundan$2) (column near3 (address signal select)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 16:38
S13	105	S12 and (delay same ((timing tim$3) (data near5 strob$3)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 16:46
S14	73	S13 and (column near3 select$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 16:48
S15	0	S14 and (redundan$4 near3 check)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 16:51
S16	0	S14 and (redundan$4 near3 check$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 16:49

S17	15	S14 and (redundan$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 17:03
S18	12	S17 and (memory near3 cell near5 array)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 17:05
S19	10	S18 and ((latch$3 trap$4) near5 signal)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 17:06
S20	10	S19 and (read$3 writ$3 I/O input output)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/15 17:07
S21	10	S20 and (method usable memory device receiv$3 data strob$3 signal memory bus captur$3 data associat$3 writ$3 command memory bus synchronization data strobe signal perform$3 column redundancy check response address associat$3 write command synchroniz$3 begin$4 internal$2 write operation memory cell array memory device clock signal method usable a memory device comprising receiving first signals indicative address associated write command latch$3 data associated writ$3 command response data strob$3 signal$3 decod$3 address produc$3 column address provid$3 column select$3 signals indicat$3 column address memory cell array memory device delay$3 delaid initiat$3 providing column select signals accommodat$3 variation timing data strobe signal perform$3 column redundancy check prior initiation providing column select signals)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 11:45

S22	9	(column adj redundancy adj check)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 11:35
S23	9	S22 and (method usable memory device receiv$3 data strob$3 signal memory bus captur$3 data associat$3 writ$3 command memory bus synchronization data strobe signal perform$3 column redundancy check response address associat$3 write command synchroniz$3 begin$4 internal$2 write operation memory cell array memory device clock signal method usable a memory device comprising receiving first signals indicative address associated write command latch$3 data associated writ$3 command response data strob$3 signal$3 decod$3 address produc$3 column address provid$3 column select$3 signals indicat$3 column address memory cell array memory device delay$3 delaid initiat$3 providing column select signals accommodat$3 variation timing data strobe signal perform$3 column redundancy check prior initiation providing column select signals)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/16 11:46